



PSU - Pulse Synch Unit



The **Pulse Synchronization Unit (PSU)** is a signaling control unit, designed for advanced synchronization, devices/units triggering, high speed pulse chains and arbitrary remote control applications. By means of its integrated **Field-Programmable Gate Array (FPGA)** it acts as a master control unit capable of generating high speed pulse chains with exceptional accuracy for signaling, **advanced timing, system level synchronization, and remote-control applications** within high-performance and demanding RF subsystems.

For high speed control and demanding RF systems, the PSU is capable of generating Low-Voltage Differential Signaling (LVDS) pulse chains using its FPGA-based architecture and distributing them through four independent output ports over standard shielded CAT5 cabling to remote peripheral boards.

Each port drives 4 synchronized LVDS pulse chains, which are converted by the Peripheral Boards into Transistor-Transistor Logic (TTL) signals for local high speed RF devices control. Configuration and control are performed via Ethernet using Transmission Control Protocol / Internet Protocol (TCP/IP) through MVG software or via standard Application Programming Interface (API). The PSU is available with battery backup option, allowing continued operation during power interruption.

APPLICATIONS

- Antenna Measurement Ranges
- Active Phased Array Calibration
- RCS (Radar Cross Section) Measurement
- Automated Test Equipment (ATE)
- Distributed Control Systems
- Payload Measurement

PRODUCT HIGHLIGHTS

- Precision pulse generation
- High-speed LVDS signals
- High-Resolution Timing: 2.5ns signal edge control (resolution)
- Flexible Signal Routing
- Versatile I/O Interface
- Remote Connectivity
- Robust Power Management

+ System Overview



1 24 V DC Power Input

A robust, industrial-grade circular connector designed for secure 24V DC power delivery. This locking interface prevents accidental power loss during vibration or critical operation, ensuring continuous uptime for mission-critical measurements.

2 USB Type-C

A modern, reversible USB Type-C port located on the front panel.

3 Network Command Interface (Ethernet / LAN)

- Standard RJ45 Ethernet port enabling full TCP/IP remote control.
- This interface allows the unit to function as a network-attached peripheral, facilitating seamless integration into distributed ATE (Automated Test Equipment) systems and remote antenna ranges.

4 Discrete I/O Interface (26-Pin High-Density D-Sub)

- A high-density (HD-26) connector providing centralized access to 16 isolated channels (8 inputs/8 outputs).
- The locking D-Sub form factor ensures signal integrity for external device triggering and state control, compliant with RS422 standards.

5 Discrete I/O Output Ports (LVDS)

4 x RJ45 ports containing 12 bidirectional optically isolated (Sink / Source) Differential Input / Output ports

6 High Speed LVDS Pulse Chains

4 x RJ45 ports each containing 4 (A, B, C, D) pulse chains

+ Specifications - PSU

PARAMETER	MODEL
	PSU

OPERATIONAL

Processor / FPGA	<ul style="list-style-type: none"> • Xilinx Zynq
Memory	<ul style="list-style-type: none"> • DDR3, QSPI Flash
System Function	<ul style="list-style-type: none"> • FPGA-based pulse and control generation • Master controller for up to 4 remote Peripheral Boards • Local or remote operation via Ethernet (TCP/IP)
Pulse Generation	<ul style="list-style-type: none"> • 4 independent LVDS output ports (RJ45) • 4 synchronized LVDS pulse chains per port (Signals A, B, C, D) • Maximum output frequency: up to 5 MHz • Timing resolution: 2.5 ns edge placement • Minimum pulse width: 10 ns • Internal logic clock: 400 MHz
Timing & Synchronization	<ul style="list-style-type: none"> • Pulse generation with nanosecond-level alignment • Independent control of multiple synchronized pulse chains • Suitable for distributed RF control architectures
Software Control	<ul style="list-style-type: none"> • MVG proprietary software • Standard API for external system integration

ELECTRICAL

Input Power	<ul style="list-style-type: none"> • Industrial grade circular 4 connector 24 V DC nominal • External 3.7 V Li-Ion battery support (JST connector) • Integrated battery charger and automatic switchover • Backup operation: >10 minutes during power loss
Differential I/O Output Ports (LVDS)	<ul style="list-style-type: none"> • 4 x RJ45 ports containing 12 bidirectional optically isolated (Sink / Source) Differential Input / Output ports
High Speed LVDS Pulse Chains	<ul style="list-style-type: none"> • 4 x RJ45 ports each containing 4 (A,B,C,D) pulse chains
Discrete I/O	<ul style="list-style-type: none"> • 26-pin high-density D-Sub connector (locking) • 8 optically isolated inputs <ul style="list-style-type: none"> - Voltage range: 5 V to 28 V DC - Response time: <1 ms - NPN / PNP compatible • 8 optically isolated outputs (sink/source) <ul style="list-style-type: none"> - Voltage: 5 V to 28 V DC - Current: 500 mA (sink) / 300 mA (source)
LVDS Output Ports	<ul style="list-style-type: none"> • 4 x RJ45, shielded, right-angle • Each port carries 4 differential LVDS pairs (A, B, C, D)

PHYSICAL

Dimensions	• 125 mm x 80 mm x 106 mm
Weight	• 0.6 Kg
Mounting Interface	• DIN Rail Mounting Fixing

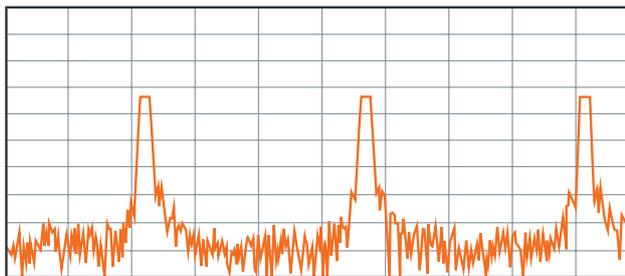
PINS ASSIGNMENT

Differential I/O (per port)	<ul style="list-style-type: none"> • 1 - 5V_Con • 2 - GND • 7,8 - DIF_IO#1 • 3,6 - DIF_IO#2 • 4,5 - DIF_IO#3
High Speed LVDS Pulse Chains RJ45 (per port)	<ul style="list-style-type: none"> • 1,2 - Signal D (+/-) • 5,4 - Signal C (+/-) • 3,6 - Signal B (+/-) • 7,8 - Signal A (+/-)
Discrete I/O Pin Summary (26-pin D-Sub)	<ul style="list-style-type: none"> • Pins 1–4, 10–13: Opto-isolated inputs (1–8) • Pins 6–9, 15–18: Opto-isolated outputs (1–8) • Pins 5, 14: 5 V reference • Pins 19–20: Input common • Pins 23–26: Output common (power/return)

ENVIRONMENTAL

Operating Temperature	• 0 °C to +50 °C (industrial grade)
Storage Temperature	• -40 °C to +85 °C

Example of MVG PSU in RF Signal Pulsing application
Scale/Div: 200nsec



Example of MVG PSU arbitrary pulse chains generation
Scale/Div: 100nsec

